I CLAIM:

1. A memory control system comprising:

a memory controller

a memory device connected to said memory controller via a command bus, wherein command signals are directed from said memory controller to said memory device, said memory device comprising:

several memory banks;

a bank refresh indicator register;

a command decoder that is connected to said bank refresh indicator and receives said command signals and controls the contents of said bank refresh indicator register; and

a refresh circuit connected to said several memory banks and said bank refresh indicator register, wherein said refresh circuit avoids unnecessary power consumption for refreshing particular ones of said several memory banks with irrelevant contents.

2. The memory control system of claim 1, wherein said refresh circuit refreshes said several memory banks only if said several memory banks contain data that was written therein.

3. The memory control system of claim 1, wherein said memory controller comprises a normal refresh circuit that sends an autorefresh signal to said memory device via said command bus.

4. The memory control system of claim 1, wherein said refresh circuit comprises:

a refresh address counter for incrementing a row address to be refreshed during a refresh cycle; and

a controller that controls access to a row address requested to be refreshed by a refresh request.

5. The memory control system of claim 1, wherein said bank refresh indicator register comprises one bit for each corresponding one of said several memory banks of said memory device, wherein said bit has a value that indicates whether or not a corresponding one of said several memory banks has to be refreshed during a refresh operation.

6. The memory control system of claim 5, wherein said bit has a value that indicates whether or not said corresponding memory bank has data that was written therein.

7. The memory control system of claim 6, wherein said decoder performs decoding of said commands and their bank-addresses and sets said value of said bit dependent on said decoding.

8. The memory control system of claim 1, wherein said refresh circuit monitors said bank refresh indicator register and starts an

activate/precharge sequence for one of said several memory banks when said bit is set to a high-level.

9. The memory control system of claim 8, wherein said refresh circuit monitors said bank refresh indicator register only in case of a self-refresh mode.

10. The memory control system of claim 8, wherein said refresh circuit monitors said bank refresh indicator register in both a self-refresh mode and auto-refresh mode.

11. The memory control system of claim 5, wherein said refresh operation is an autorefresh operation.

12. The memory control system of claim 5, wherein said refresh operation is a self-refresh operation.

13. The memory control system of claim 1, wherein said memory controller comprises a normal refresh circuit.

14. The memory control system of claim 1, wherein said bank refresh indicator register is programmable.

15. A method of refreshing several memory banks that receive command signals from a memory controller, the method comprising:

monitoring command signals received by a memory device; and

refreshing said several memory banks based on said monitored command signals so as to avoid unnecessary power consumption for refreshing particular ones of said memory banks with irrelevant contents.

16. The method of claim 15, wherein said monitoring comprises determining whether or not a write command is received by said memory device and indicating that one of said several memory banks contains data stored therein.

17. The method of claim 15, wherein said refreshing is a self-refreshing operation.

18. The method of claim 15, wherein said refreshing is an auto-refreshing operation.

19. The method of claim 15, further comprising setting a bit of a bank refresh indicator register to a value dependent on said monitoring; and

wherein said refreshing of said several memory banks is dependent on said value of said bit.

20. The method of claim 19, wherein said bit is reset to a low value at power-up of said several memory banks.

21. The method of claim 19, wherein said refreshing is performed if said value of said bit is high.

22. The method of claim 19, wherein said refreshing is not performed if said value of said bit is low.

23. The method of claim 19, wherein said monitoring comprises:

decoding any write command issued to said memory device; and

decoding a bank-address to which data is written.

24. The method of claim 23, further comprising setting said bit to a high level.

25. The method of claim 23, further comprising resetting said bit to a low level via a special command sequence, usually referred to as extended mode register set.